REMARKS

This paper is being provided in response to the Office Action dated September 2, 2003, for the above-referenced application and *supplements* the Response previously filed on November 25, 2003. In this supplemental response, Applicant has cancelled claims 25 and 26 without prejudice or disclaimer of the subject matter thereof, amended claim 27 and added new claims 29-31 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims and the new claims are fully supported by the originally filed application.

Applicant has not further amended the specification herein but notes that the Response filed on November 25, 2003, contains amendments to the specification for purposes of clarification.

Applicant thanks the Examiner for allowing claims 15 and 22-24 and for the indication of allowable subject matter in claim 20. In the Response filed on November 25, 2003, Applicant rewrote claim 20 into independent form to incorporate the base claim and any intervening claims. Applicant respectfully submits that claim 20 is in condition for allowance.

The rejection of claim 25 under 35 U.S.C. 112, first paragraph, is hereby traversed. The Office Action states that the feature of "a NOR gate receiving the logic signal and the output signal" is not supported in the specification or drawings as originally filed. As noted in the Response filed on November 25, 2003, Applicant respectfully submits that elements V43 and V45 are shown as NOR gates in originally-filed Figure 4 but incorrectly identified as NAND

gates in the specification. Applicant previously amended the specification to correct this error and to bring the specification and drawing into conformance with one another. Although Applicant has cancelled claim 25 herein, Applicant respectfully refers to the above-noted remarks insofar as new claim 29 contains a feature that includes a NOR gate.

The rejection of claims 19, 21, 27 and 28 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,055,713 to Watanabe et al. (hereinafter "Watanabe") is hereby traversed and reconsideration is respectfully requested.

Independent claim 19, as amended in the Response filed November 25, 2003, recites a delay circuit. The circuit includes first and second nodes and first and second inverters. The first inverter receives a logic signal and its output is coupled to the first node. The input of the second inverter is coupled to the first node and the output is coupled to the second node. A first capacitor is coupled between the first node and a first power source line, the first capacitor being a first transistor of a first channel type. The second capacitor is coupled between the second node and a second power source line different from the first power source line, the second capacitor being a second transistor of a second channel type different from the first channel type. Further, when the logic signal is fixed at a low level during a standby state, one of the first capacitor and the second capacitor is set to an off-state in response to a chip select signal controlling the standby state, and the other of the first capacitor and the second capacitor is set to an off-state in response to the chip select signal that is negated. Claim 21 depends on independent claim 19.

Independent claim 27, as amended herein, recites a delay circuit receiving a logic signal having a first logical level and a second logical level. An inverter chain is included including a plurality of inverters and at least one first capacitor, the inverter chain receiving a logic signal. The first capacitor includes a MOS transistor of a first channel type. The capacitor is operated to increase and decrease capacitance based on changes in the logical levels of the logic signal and whereby a first delay signal and a second delay signal are generated, the second delay time being shorter than the first delay time. A logical gate receives the output of the inverter chain and the logic signal so that the logical gate outputs its output signal in response to the first delay signal when the logic signal changes from the first logical level to the second logical level. Claim 28 depends on independent claim 27.

The Watanabe reference discloses an output circuit of an integrated circuit including first and second MOS transistors and a drive and control circuit. In Fig. 5, Watanabe discloses two inverters (I2 and I3), two capacitors (C1 and C2) and power source lines (VSS and VCC) with an output directed to a logic gate (a NAND gate-NA1).

Applicant's independent claim 19 recites at least the feature that when the logic signal is fixed at a low level during a standby state, one or more capacitors are set to an off-state in response to a chip select signal controlling the standby state. In structures based on MOS capacitors or inverters comprising MOS transistors, generation of leak current during the standby state is suppressed and thereby source-voltage dependency of the delay time is contained and power consumption is effectively controlled during the standby state. (See Figure 10 and page 32, line 2 to page 33, line 4 of the present application).

Applicant respectfully submits that Watanabe does not teach or fairly suggest at least the above-noted features as claimed by Applicant. Watanabe does not disclose the circuit configuration as claimed by Applicant including capacitors that comprise MOS transistors and wherein when the logic signal is fixed at a low level during a standby state, one or more capacitors are set to an off-state in response to a chip select signal controlling the standby state. Accordingly, Applicant respectfully requests that the rejection of claim 19 be reconsidered and withdrawn.

Further, with respect to Applicant's independent claim 27, Fig. 5 of Watanabe discloses a delay circuit with a NAND gate NA1 and Figs. 7 and 11 of Watanabe disclose the delay circuit with a NOR gate NG. Regarding the inverted signal of signal C in Fig. 5, the rising edge is targeted for delay. On the rising of the inverted signal, the output signal of the inverter I2 falls and the output signal of the inverter I3 rises. Because the MOS capacitor C2 is supplied with the Vcc, it is a p-type MOS capacitor. Therefore, on the rising of the inverted signal, the MOS capacitors C1 and C2 are supplied with the signal so that their capacitance *decreases*. (See Figs. 5, 7 and 11 of Watanbe and timing diagrams showing delay in the Appendix attached hereto.)

In contrast, because the present invention makes a delay by *increasing* the capacitance, it differs from the delay circuit shown in Fig. 5 of Watanabe. The delay circuit shown in Figs. 7 and 11 of Watanabe also operates so that the capacitance of the capacitor in the delay circuit *decreases* when the level of the logic signal supplied to the delay circuit becomes the targeted

level. Accordingly, in view of the above, Applicant respectfully requests that the rejection of claim 27 be reconsidered and withdrawn.

Further, Applicant has added new claims 29-31 and respectfully submits that these claims are allowable over the prior art of record, as noted in detail below.

In Fig. 5 of Watanabe, the delay circuit with the NAND gate NA1 comprises three nodes and two inverters. The first node is supplied with the logical signal and the third node is connected to the NAND gate NA1. That is, the delay circuit shown in Fig. 5 of Watanabe comprises the inverter chain having (2n+1) nodes and 2n inverters. The first node is supplied with the logical signal and the (2n+1)-th node is connected to the NAND gate NA1. In light of the above operations, an n-MOS capacitor is connected to *an even node* and a p-MOS capacitor is connected to *an odd node*. (See illustrations in the Appendix attached hereto.)

In contrast, in the present invention, as shown in Fig. 6 of the present application, the delay circuit with NAND gate comprises the delay system D62. The delay system D62 comprises the inverter chain having (2n+1) nodes and 2n inverters. As indicated in Fig. 1A, the first node is supplied with the logical signal and the (2n+1)-th node is connected to the NAND gate. Moreover, in the present invention, an n-MOS capacitor is connected to *an odd node* and a p-MOS capacitor is connected to *an even node*. Therefore, the delay circuit with a NAND gate according to the present invention differs from the delay circuit shown in Fig. 5 of Watanabe. (See illustrations in the Appendix attached hereto.)

Next, as indicated in Fig. 6 of the present application, the delay circuit with an AND gate according to the present invention comprises the delays system D61. The construction of the delay system D61 is the same as that of the delay system D62 (see Fig. 1A of the present application). Therefore, the delay circuit with the AND gate according to the present invention differs from the delay circuit shown in Fig. 5 of Watanabe.

Next, as indicated in Fig. 4 of the present application, the delay circuit with NOR gate according to the present invention comprises the inverter chain (2n+1) nodes and 2n inverters. The first node is supplied with the logical signal and the (2n+1)-th node is connected to the NOR gate. Moreover, in the present invention, an n-MOS capacitor is connected to *an even node*. In contrast, in the delay circuit with the NOR gate NG shown in Figs. 7 and 11 of Watanabe, an n-MOS capacitor is connected to *an odd node*. Therefore, the delay circuit with the NOR gate according to the present invention differs from the delay circuit shown in Watanabe.

Based on the above, applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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